Subt B1 **In the Claims:**

A3

1. (Amended) A semiconductor device having an input/output protection circuit section on a semiconductor substrate, wherein:

said input/output protection circuit section comprises a plurality of field effect transistors connected in parallel, each of which has a first diffusion layer of a first conductive type and a second diffusion layer of the first conductive type and a gate electrode that is disposed between said first and second diffusion layers;

a dopant diffusion region of a second conductive type that is set at a distance from said plurality of field effect transistors;

wherein said dopant diffusion region is connected to a reference potential, and wherein the second diffusion layer is connected to an input/output terminal section; and

wherein under the first diffusion layer, there is formed a first conductive type well with a lower dopant concentration than the first diffusion layer.

Subt C1

2. (Amended) The semiconductor device according to Claim 1, wherein said gate electrode and said dopant diffusion region of second conductive type are disposed over a second conductive type well that is formed on the surface of the semiconductor substrate; and wherein the bottom of said first conductive type well is formed at the same depth as the bottom of the second conductive type well or at a level deeper than the bottom of the second conductive type well.

Subt B2

3. (Amended) The semiconductor device according to Claim 1, wherein said plurality of field effect transistors are N-channel type field effect transistors.

4. (Amended) A semiconductor device having, on a semiconductor substrate, an input/output protection circuit section that contains a complementary field effect transistor, wherein:

said complementary field effect transistor comprises a first field effect transistor having a first diffusion layer of first conductive type, a second diffusion layer of first conductive type, and a gate electrode that is disposed between these layers and a second field effect transistor having a third diffusion layer of second conductive type, a fourth diffusion layer of second conductive type, and a gate electrode that is disposed between these layers;

A3 end

wherein a first dopant diffusion region of second conductive type is set at a distance from said first field effect transistor, and a second dopant diffusion region of first conductive type is set at a distance from said second field effect transistor;

wherein the first dopant diffusion region is connected to a first reference potential, the second dopant diffusion region is connected to a second reference potential, and the second diffusion layer and the fourth diffusion layer are each connected to an input/output terminal section; and

wherein under the first diffusion layer, there is formed a first conductive type well with a lower dopant concentration than the first diffusion layer.

Amd C1

5. (Amended) The semiconductor device according to Claim 4, wherein the gate electrode of the first field effect transistor and the first dopant diffusion region are disposed over a second conductive type well that is formed on the surface of the semiconductor substrate; and

wherein the bottom of said first conductive type well is formed at the same depth as the bottom of the second conductive type well or at a level deeper than the bottom of the second conductive type well.

6. (Amended) The semiconductor device according to Claim 5, wherein, beneath the second conductive type well, there is set a dopant high-concentration region containing second conductive type dopants with a higher dopant concentration than the second conductive type well; and

wherein the bottom of said first conductive type well is formed at the same depth as the bottom of said dopant high-concentration region or at a level deeper than the bottom of said dopant high-concentration region.

7. (Amended) The semiconductor device according to Claim 4, wherein the first field effect transistor is an N-channel type field effect transistor.

Add Subt B3

8. (New) A semiconductor device having an input/output protection circuit section on a semiconductor substrate, wherein:

said input/output protection circuit section comprises a plurality of field effect transistors connected in parallel, each of which has a first diffusion layer of a first

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conductive type and a second diffusion layer of the first conductive type and a gate electrode that is disposed between said first and second diffusion layers;

a dopant diffusion region of a second conductive type that is set at a distance from said plurality of field effect transistors;

wherein said dopant diffusion region is connected to a reference potential, and wherein the second diffusion layer is connected to an input/output terminal section;

wherein under the first diffusion layer, there is formed a first conductive type well with a lower dopant concentration than the first diffusion layer; and

wherein the first conductive type well at least partially underlies an element isolation film.